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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,200	04/11/2001	Chul-Min Kim	P56349	1160

7590 10/03/2006

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EXAMINER	
SHIBRU, HELEN	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,200	KIM, CHUL-MIN	
	Examiner	Art Unit	
	HELEN SHIBRU	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered and the last Office Action is withdrawn. However, upon further consideration, the arguments are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

2. The indicated allowability of claims 8-9 and 18-19 are withdrawn in view of the newly discovered reference(s). The Examiner regrets any inconvenience this might have caused and non Final Office action based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being obvious over Jeong (US Pat. No. 5,218,489) in view of Official Notice and further in view of Gedl (US Pat. No. 6,185,359).

Regarding claim 1, Jeong discloses a video signal processing with an envelope detector (see fig. 2 and 3 envelope detector (200)) for detecting and outputting an envelope of a frequency modulated (FM) video signal (see col. 2 lines 26-33, col. 3 lines 52-65 and claims 1-6);

a level variation switching circuit (see fig. 3 comparator (300), second amplifier (450), and microcomputer (400)) for changing an envelope level of the FM video signal (the video

signal detected by the reproducing head HD and that supplies to the comparator (300) then to microcomputer (400). See col. 3 lines 41-65).

Claim 1 differs from Jeong in that the claim further requires a video signal processing integrated circuit (IC) having the envelope detector. Although Jeong does not specifically said the circuit is integrated, Jeong discloses the circuit includes transistors, capacitors, resistors and diodes. Official Notice is given that it is well known in the art to integrate circuit using the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jeong by using integrated circuit in order to reduce system complexity, cost and transmitter performance.

Claim 1 further differs from Jeong in that the claim further requires connecting an input of the level variation switching circuit to a control output of a microprocessor. Official Notice is taken that whether the same apparatus is constructed in one element or in two elements by doing so produces novel and/or unexpected results is merely considered as well known design options obvious to one of ordinary skill in the art because the construction of the apparatus provides no significant functional or patentable difference on the same taken ~~taken~~ that separating the same apparatus into three or more elements would have been patentable distinct from the applicant's apparatus. The Applicant agreed that the microcomputer 400 should be a part of the level variation switching circuit, and therefore the three elements together vary the level of the output signal. See court decision Nerwin v. Erlichman 168 USPQ 177.

TTP 9/26/06

Claim 1 further differs from Jeong in that the claim further requires ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from the microprocessor.

In the same field of endeavor Gedl discloses an envelope detector to detect the envelopes of the color television signals, reproduced by means of one of the two magnetic heads SP-K1 and SP-K2 and one of the other two magnetic heads LP-K1 and LP-K2, applied to it and to generate envelope information as detection information which indicates whether the envelope of the color television signal, the SP or the LP, has a larger amplitude (see col. 9 lines 40-55). Gedl further discloses the microcomputer 19 has an output connected to a control input 52 of the head switching stage 49 (see fig. 1 and col. 8 lines 32-56). Therefore in light of the teaching in Gedl it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jeong by providing a switch, which can be On/Off, based on the detected envelope signal in order to select one of the modes.

Regarding claims 2 and 3, claims 2 and 3 differ from Jeong in that the claims further requires that standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microcomputer, and the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder. Although Jeong does not specify standard playback (SP) mode information and super long playback (SLP) mode information contained in the control data input from the microcomputer, and the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder, Jeong discloses in the microcomputer 400 the output signal is stepped up or down based on the duty ratio difference. Jeong further discloses the switch SW1 selects automatic or manual tracking control (see col. 2 lines 58-62). Jeong further discloses the apparatus is effective tracking control for speed varying reproduction such as

slow -motion reproduction (see col. 1 lines 13-17 and col. 1 lines 26-32). Jeong further teaches PAL type width (see col. 3 lines 17-21).

Gedl discloses the signal is varying according to SP and LP mode (see rejection of claim 1 above). Gedl further discloses the output terminal of 49 is connected to the recording/reproducing switch 66.

However claim 2 differ from Jeong and Gedl in that the playback mode includes SLP mode. Although Gedl does not specify that the SP and SLP mode, Gedl discloses SP and LP mode. Official Notice is taken that it is well known in the art to use SLP mode. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SLP mode in order to provide better recording quality.

Regarding claim 4, claim 4 differs from Jeong in that the claim further requires the level variation switching circuit has a resistor at an output terminal of the envelope detector. Although Jeong and Gedl does not specifically said a resistor at an output terminal of the envelope detector Jeong discloses a waveform shaper includes resistors. Official Notice is taken that it is well known in the art and it is a designer choice at the time the invention was made to add a resistor at the output terminal of the envelope detector in the level varying switching circuit. Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to add a resistor in order to reduce the load since the input voltage is known.

Regarding claim 5, Jeong discloses a video signal processing circuit incorporating an envelope detecting circuit (see fig. 3 envelope detector (200)) for detecting an envelope level of an FM video signal (see col. 2 lines 26-33), wherein the envelope detecting circuit comprises:

a peak detector (see fig. 3 inside waveform shaper (230) D2, R7 and C5, and the band pass filter (220) and fig. 4) for receiving the FM video signal and for detecting a peak value of the FM video signal (see col. 1 lines 52-67, col. 2 lines 47-53, col. 3 lines 27-55 and claims 1-12, waveform shaping); and

a level switch (see fig. 3 second amplifier (450) and comparator (300) and microcomputer (400)) having a first input connected to an output of the peak detector (see fig. 2 and col. 2 lines 29-38 and col. 3 lines 7-15. See also col. 3 lines 41-65).

Claim 5 differs from Jeong in that the claim further requires a level switch having a second input connected to a control output of a microprocessor for controlling the envelope level of the FM video signal according to mode information applied from the microprocessor. Official Notice is taken that whether the same apparatus is constructed in one element or in two elements by doing so produces novel and/or unexpected results is merely considered as well known design options obvious to one of ordinary skill in the art because the construction of the apparatus provides no significant functional or patentable difference on the same ~~taken~~ taken that separating the same apparatus into three or more elements would have been patentable distinct from the applicant's apparatus. The Applicant agreed that the microcomputer 400 should be a part of the level variation switching circuit, and therefore the three elements together vary the level of the output signal. The peak detector is connected to the level variation circuit (elements 300, 450 and 400). See court decision Nerwin v. Erlichman 168 USPQ 177.

Regarding claim 6, Jeong discloses an amplifier (see fig. 3 first amplifier (210)) connected to an input terminal of the peak detector for amplifying the FM video signal with a predetermined gain prior to provision to the peak detector (see col. 3 lines 27-34).

Regarding claim 7, although Jeong does not specify that an amplifier connected to an output terminal of the peak detector for amplifying the FM video signal with a predetermined gain after processing in the peak detector, Jeong does disclose the head switching pulse is supplied to the input port I1 of the microcomputer with the result that the pulse train A having a predetermined number of pulses for every period (see col. 3 lines 7-15). Official Notice is given that it is well known in the art that connecting an amplifier with an output terminal of the peak detector. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jeong by providing an amplifier connected to an output terminal of the peak detector in order to control the gain.

Regarding claims 8 and 18, Jeong discloses a video signal processing circuit incorporating an envelope detecting circuit (see fig. 3 envelope detector (200)) for detecting an envelope level of an FM video signal (see col. 2 lines 26-33), wherein the envelope detecting circuit comprises:

a peak detector (see fig. 3 inside waveform shaper (230) D2, R7 and C5, and the band pass filter (220) and fig. 4) for receiving the FM video signal and for detecting a peak value of the FM video signal (see col. 1 lines 52-67, col. 2 lines 47-53, col. 3 lines 27-55 and claims 1-12, waveform shaping); and

a level switch (see fig. 3 second amplifier (450) and comparator (300) and microcomputer (400)) having a first input connected to an output of the peak detector (see fig. 2 and col. 2 lines 29-38 and col. 3 lines 7-15. See also col. 3 lines 41-65).

Claims 8 and 18 differs from Jeong in that the claim further requires a level switch having a second input connected to a control output of a microprocessor for controlling the

envelope lev el of the FM video signal according to mode information applied from the microprocessor. Official Notice is taken that whether the same apparatus is constructed in one element or in two elements by doing so produces novel and/or unexpected results is merely considered as well known design options obvious to one of ordinary skill in the art because the construction of the apparatus provides no significant functional or patentable difference on the same ~~taken~~ token that separating the same apparatus into three or more elements would have been patentable distinct from the applicant's apparatus. The Applicant agreed that the microcomputer 400 should be a part of the level variation switching circuit, and therefore the three elements together vary the level of the output signal. The peak detector is connected to the level variation circuit (elements 300, 450 and 400). See court decision Nerwin v. Erlichman 168 USPQ 177.

TTQ 9/27/06

Claims 8 and 18 further differ from Jeong in that the claims further require a resistance elemnt having a first terminal connected to the output of the peak detector and having a second terminal connected to the switching control element. Although Jeong does not specifically disclose a resistance element having a first terminal connected to the output of the peak detector and having a second terminal connected to the switching control element, Jeong discloses a waveform shaper includes resistors. Official Notice is taken that it is well known in the art and it is a designer choice at the time the invention was made to add a resistor at the output terminal of the peak detector in the level varying switching circuit. Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to add a resistor in order to reduce the load since the input voltage is known.

Claims 9 and 19 are rejected for the same reason as discussed in claim 3 above.

Claim 10 is rejected for the same reason as discussed in claims 2 and 3 above.

Regarding claim 11, the limitations of claim 11 can be found in claims 1, 2 and 3. Therefore claim 11 is analyzed and rejected for the same reasons as discussed in claims 1, 2, and 3.

Regarding claims 12-13, the limitation of claims 12-13 can be found in claims 2 and 3. Therefore claim 12-13 are analyzed and rejected for the same reasons as discussed in claims 2 and 3.

Claim 14 is rejected for the same reason as described in claim 4 above.

Claim 15 is rejected for the same reason as described in claim 5 above.

Claim 16 is rejected for the same reason as described in claim 6 above.

Claim 17 is rejected for the same reason as described in claim 7 above.

Claim 20 is rejected for the same reason as described in claims 2 and 3 above.

5. Claims 1-4, and 10-14 are rejected under 35 U.S.C. 103(a) as being obvious over Jeong in view of Choi (US Pat. No. 5,519,549).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in

the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 1, Jeong discloses a video signal processing with an envelope detector (see fig. 2 and 3 envelope detector (200)) for detecting and outputting an envelope of a frequency modulated (FM) video signal (see col. 2 lines 26-33, col. 3 lines 52-65 and claims 1-6);

a level variation switching circuit (see fig. 3 comparator (300), second amplifier (450), and microcomputer (400)) for changing an envelope level of the FM video signal (the video signal detected by the reproducing head HD and that supplies to the comparator (300) then to microcomputer (400). See col. 3 lines 41-65).

Claim 1 differs from Jeong in that the claim further requires a video signal processing integrated circuit (IC) having the envelope detector. Although Jeong does not specifically said the circuit is integrated, Jeong discloses the circuit includes transistors, capacitors, resistors and diodes. Official Notice is given that it is well known in the art to integrate circuit using the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jeong by using integrated circuit in order to reduce system complexity, cost and transmitter performance.

Claim 1 further differs from Jeong in that the claim further requires connecting an input of the level variation switching circuit to a control output of a microprocessor. Official Notice is taken that whether the same apparatus is constructed in one element or in two elements by doing so produces novel and/or unexpected results is merely considered as well known design

options obvious to one of ordinar y skill in the art because the construction of the apparatus provides no significant functional or patentable difference on the same token that separating the same apparatus into three or more elements would have been patentable distinct from the applicant's apparatus. The Applicant agreed that the microcomputer 400 should be a part of the level variation switching circuit, and therefore the three elements together vary the level of the output signal. See court decision Nerwin v. Erlichman 168 USPQ 177.

Claim 1 further differs from Jeong in that the claim further requires ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from the microprocessor.

In the same field of endeavor Choi discloses a microprocessor that supplies various speed signals, SP, SLP, and LP. Choi further discloses transistors are turning on and off to change the voltage level needed (see cols. 4 5 and 6). Therefore in light of the teaching in Choi it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an ON/OFF switching circuit in order to change the speed.

Claims 2 and 3 are rejected for the same reason as discussed in claim 1 above.

Regarding claim 4, claim 4 differs from Jeong in that the claim further requires the level variation switching circuit has a resistor at an output terminal of the envelope detector. Although Jeong and Choi does not specifically said a resistor at an output terminal of the envelope detector Jeong discloses a waveform shaper includes resistors. Choi discloses resistors connected to the transistors to change the voltage level needed. Official Notice is taken that it is well known in the art and it is a designer's choice at the time the invention was made to add a resistor at the output terminal of the envelope detector in the level varying switching circuit. Therefore it is obvious to

one of ordinary skill in the art at the time the invention was made to add a resistor in order to reduce the load since the input voltage is known.

Claim 10 is rejected for the same reason as discussed in claims 2 and 3 above.

Regarding claim 11, the limitations of claim 11 can be found in claims 1, 2 and 3. Therefore claim 11 is analyzed and rejected for the same reasons as discussed in claims 1, 2, and 3.

Regarding claims 12-13, the limitation of claims 12-13 can be found in claims 2 and 3. Therefore claim 12-13 are analyzed and rejected for the same reasons as discussed in claims 2 and 3.

Claim 14 is rejected for the same reason as described in claim 4 above.

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gedl (US Pat. No. 6,185,359) in view of Official Notice.

Regarding claim 1, Gedl discloses an envelope detector for detecting and outputting an envelope of a frequency modulated video signal (see col. 9 lines 40-55);

Providing the video signal processing IC with a level variation switching circuit for changing an envelope level of the FM video signal (see head switching stage (49), terminals 48, 50, 53, input 52, and also elements 39, 42, 44, 45, 46, 47 and 19 in fig. 1 and figures 2 and 3, col. 9 line 55-col. 10 line 8 and col. 19 lines 38-58); and

Connecting an input of the level variation switching circuit to a control output of a microprocessor so that ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from the microprocessor (see fig. 1 and col. 8 lines 32-56).

Claim 1 differs from Gedl in that the claim further requires an FM video signal processing integrated circuit (IC) having the envelope detector. Although Gedl does not specifically said the circuit is integrated, Gedl the color signal demodulator and switching information generating have been incorporated in an integrated circuit (see col. 5 lines 6-16). Official Notice is given that it is well known in the art to integrate circuit using the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gedl by using integrated circuit in order to reduce system complexity, cost and transmitter performance.

Regarding claims 2 and 3, claims 2 differs from Gedl in that the claim further requires SPL mode. Although Gedl does not specifically disclose SPL mode Gedl discloses the signal is varying according to SP and LP mode (see rejection of claim 1 above). Official Notice is taken that it is well known in the art to substitute LP mode with SLP mode. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SLP mode in order to provide better recording quality.

Regarding claim 3, Gedl discloses the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder (see fig. 1).

Regarding claim 4, claim 4 differs from Gedl in that the claim further requires the level variation switching circuit has a resistor at an output terminal of the envelope detector. Although Gedl does not specifically disclose a resistor at an output terminal of the envelope detector, Gedl discloses the speed of the tape recorder is changing. Official Notice is taken that it is well known in the art and it is a designer's choice at the time the invention was made to add a resistor at the output terminal of the envelope detector in the level varying switching circuit. Therefore it is

obvious to one of ordinary skill in the art at the time the invention was made to add a resistor in order to reduce the load since the input voltage is known.

Claim 10 is rejected for the same reason as discussed in claims 2 and 3 above.

Regarding claim 11, the limitations of claim 11 can be found in claims 1, 2 and 3. Therefore claim 11 is analyzed and rejected for the same reasons as discussed in claims 1, 2, and 3.

Regarding claims 12-13, the limitation of claims 12-13 can be found in claims 2 and 3. Therefore claim 12-13 are analyzed and rejected for the same reasons as discussed in claims 2 and 3.

Claim 14 is rejected for the same reason as described in claim 4 above.

Regarding claim 5, Gedl discloses an envelope detecting circuit for detecting an envelope level of an FM video signal (see rejection of claim 1 above), wherein the envelope detecting circuit comprises:

A peak detector for receiving the FM video signal and for detecting a peak value of the FM video signal (the envelope detector 60 is constructed as a peak detector, see fig. 5 and fig. 1 elements 39, 42, 44, 45, 46, 47, 48, 49, 50, 52, 53, and 19 and col. 23 lines 20-38);

A level switch having a first input connected to an output of the peak detector and having a second input connected to a control output of a microprocessor for controlling the envelope level of the FM video signal according to mode information applied from the microprocessor so as to reduce a variation in the envelope level in accordance with a type of operation of a video cassette recorder (see fig. 1 elements 39, 42, 44, 45, 46, 47, 48, 49, 50, 52, 53, and 19 and col. 10 lines 23-57 col. 23 lines 3-38, and rejection of claim 1 above).

Claim 5 differs from Gedl in that the claim further requires an FM video signal processing integrated circuit (IC) having the envelope detector. Although Gedl does not specifically said the circuit is integrated, Gedl the color signal demodulator and switching information generating have been incorporated in an integrated circuit (see col. 5 lines 6-16). Official Notice is given that it is well known in the art to integrate circuit using the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gedl by using integrated circuit in order to reduce system complexity, cost and transmitter performance.

Regarding claim 6, Gedl discloses an amplifier connected to an input terminal of the peak detector for amplifying the FM video signal with a predetermined gain prior to provision to the peak detector (see fig. 1 element 2 and fig. 5).

Regarding claim 7, Gedl discloses an amplifier connected to an output terminal of the peak detector for amplifying the FM video signal with a predetermined gain after processing in the peak detector (see fig. 5).

Regarding claim 8, Gedl discloses an envelope detecting circuit for detecting an envelope level of an FM video signal (see rejection of claim 1 above), wherein the envelope detecting circuit comprises:

A peak detector for receiving the FM video signal and for detecting a peak value of the FM video signal (the envelope detector 60 is constructed as a peak detector, see fig. 5 and fig. 1 elements 39, 42, 44, 45, 46, 47, 48, 49, 50, 52, 53, and 19 and col. 23 lines 20-38);

A level switch having a first input connected to an output of the peak detector and having a second input connected to a control output of a microprocessor for controlling the envelope

level of the FM vid eo signal according to mode information applied from the microprocessor so as to reduce a variation in the envelope level in accordance with a type of operation of a video cassette recorder (see fig. 1 elements 39, 42, 44, 45, 46, 47, 48, 49, 50, 52, 53, and 19 and col. 10 lines 23-57 col. 23 lines 3-38, and rejection of claim 1 above).

Claim 8 differs from Gedl in that the claim further requires an FM video signal processing integrated circuit (IC) having the envelope detector. Although Gedl does not specifically said the circuit is integrated, Gedl the color signal demodulator and switching information generating have been incorporated in an integrated circuit (see col. 5 lines 6-16). Official Notice is given that it is well known in the art to integrate circuit using the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gedl by using integrated circuit in order to reduce system complexity, cost and transmitter performance.

Claim 8 further differs from Gedl in that the claim further requires the level variation circuit includes a resistance element having a first terminal connected to the output of the peak detector and having a second terminal connected to the switching control element. Although Gedl does not specifically disclose the above limitation, Gedl discloses the speed of the tape recorder is changing. Official Notice is taken that it is well known in the art and it is a designer's choice at the time the invention was made to add a resistor at the output terminal of the peak detector in the level varying switching circuit. Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to add a resistor in order to reduce the load since the input voltage is known.

Claim 18 is rejected for the same reason as discussed in claim 8 above.

Claim 9 and 19 are rejected for the same reason as discussed in claim 2 above.

Claim 15 is rejected for the same reason as described in claim 5 above.

Claim 16 is rejected for the same reason as described in claim 6 above.

Claim 17 is rejected for the same reason as described in claim 7 above.

Claim 20 is rejected for the same reason as described in claims 2 and 3 above.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELEN SHIBRU whose telephone number is (571) 272-7329. The examiner can normally be reached on M-F, 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, THAI Q. TRAN can be reached on (571) 272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Shibru